SnO_2 Nanowire Logic Devices on Deformable Nonplanar Substrates

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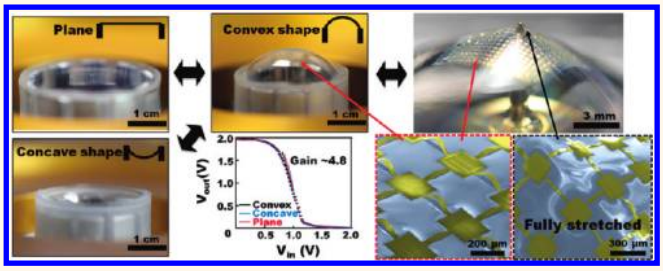
ABSTRACT



Logic inverters consisting of n-type FETs and resistors with SnO_2 nanowire channels were fabricated on films of the elastomer polydimethylsiloxane, prestrained and flattened into planar sheets from initial, preformed hemispherical shapes. Upon release, thin and narrow interconnects between individual devices in the arrays absorb induced strain by buckling into nonplanar sinusoidal shapes, to allow full recovery of the surfaces to their original convex geometries. The same physics allows deformation of convex shapes into concave ones, as well as more complex surfaces of coexisting convex and concave areas, and small regions with extremely stretched, locally tapered forms, all nondestructively achieved while maintaining electrical performance, enhanced by use of air gap gate dielectrics. This work shows, more generally, that nanowire devices with both conventional and unusual designs can be integrated into overall systems with irregular, nonplanar layouts, easily deformed in reversible fashion without any measurable alteration in electrical characteristics. The results suggest potential applicability of nanowire technologies in systems of tissue-matched implantable electronics for mounting directly on human organs or of sensor skins for integration with robotic manipulators.

KEYWORDS: deformable · elastomers · hemisphere · logic device · nanowires · stretchable

Conventional electronic devices exist on flat, rigid wafers or glass substrates. Such configurations are suitable for many existing applications, but are they incompatible with use in deformable layouts or on complex curved surfaces, as required for devices designed to mount on human skin or internal organs. This constraint limits potential applications in medical monitoring systems and in devices for prosthetic control. Several examples of high-performance stretchable technologies have been reported for nonplanar systems that incorporate inorganic materials in nanomembrane formats.[1,2] Examples include hemispherical/paraboloid electronic eye cameras,[3−7] curvilinear electronics,[8] stretchable inorganic LEDs,[9] displays,[10] photovoltaics,[11] sensors,[12] logic devices using thin Si material,[13,14] biointegrated devices,[15−18] and biocompatible sensor-assisted medical instruments.[19]

Nanowires (NWs) are expected to aid the development of these and other stretchable electronic systems by improving performance, expanding integration possibilities, opening up new modes of operation, and potentially lowering cost by virtue of superior electronic/optical properties, high aspect ratios, large surface areas, and compatibility with bulk synthesis.[20,21] Nanowires also create unique opportunities in chem/biosensors and other classes of advanced semiconductor devices that cannot be addressed using other classes of nanomaterials. Among the many materials that have been explored in NW formats, SnO_2 is particularly promising, due to its ease of synthesis and its demonstrated applications in optoelectronic and sensor components with n-type semiconducting properties, direct band gap energies of 3.6 eV, and high sensitivity to surface adsorption of various gas molecules.

Here, we report on the fabrication of transistors and inverters that use freely suspended, aligned arrays of SnO_2 NWs as active materials, integrated on membranes of polydimethylsiloxane, prestrained and flattened into planar forms from initial, preformed hemispherical shapes. Changes in the geometries of thin, narrow interconnects enable strain accommodation without significant deformation of the suspended NWs in the devices, as confirmed

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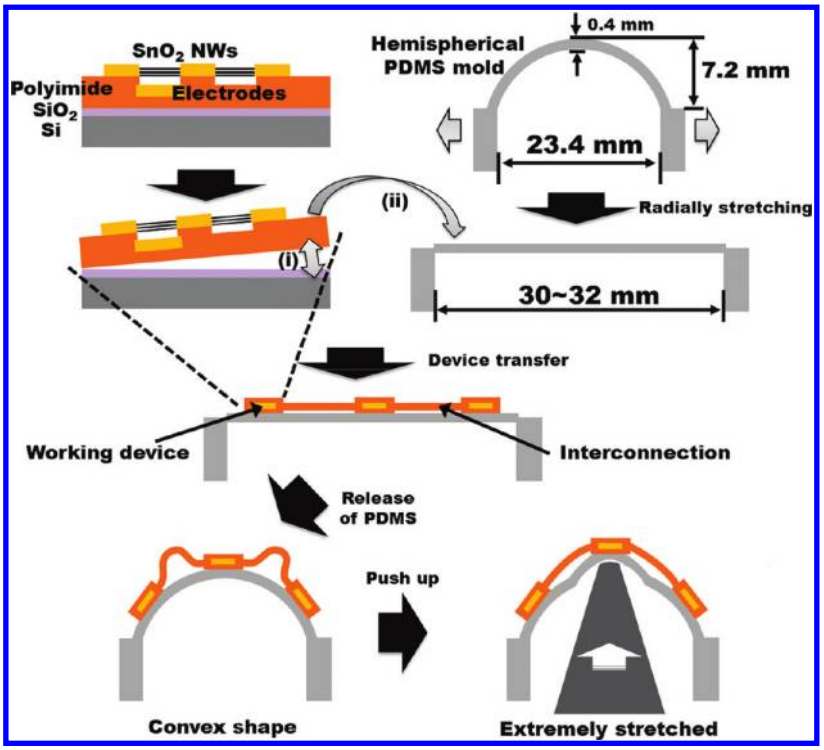

Figure 1. Schematic illustration of steps for fabrication of NW inverter arrays on a hemispherical substrate. (i) Detachment of the PI layer from a SiO_2/Si substrate using an adhesive tape and (ii) placing the detached devices onto the PDMS film, flattened by a stretching stage.

by quantitative mechanics modeling. We illustrate the operational characteristics and the mechanics through test platforms that are capable of dynamic strains to yield complex shapes, including both concave and convex domes, sharp pinpoint protrusions, and combined configurations of both positive and negative curvature accomplished by application of external local force. In particular, the NW channel region remained unchanged without noticeable disturbance under such extreme deformations, resulting in stable, invariant transfer characteristics of SnO_2 NW transistors. These results not only extend the sorts of capabilities previously demonstrated with nanomembranes but they also illustrate compatibility with NW systems, where measurements show that the electrical properties of field effect transistors (FETs) and inverters (field effect mobility of *ca.* 80 $cm^2/(V \cdot s)$, threshold voltages of *ca.* 0.7 V, and maximum input−output gains of *ca.* 4.8) remain insensitive to overall system shape.

RESULTS AND DISCUSSION

Figure 1 outlines the fabrication of a NW inverter array on a film formed into a hemisphere shape with convex curvature and that with sharp pinpoint protrusion. Thin polyimide (PI) films (*ca.* 300 nm) were prepared by spin-coating diluted poly(amic acid) (Aldrich) onto SiO_2 substrates, following a three-stage curing recipe: 95 °C for 3 min, 150 °C for 10 min, and 250 °C for 2 h under Ar atmosphere. Both the resistors

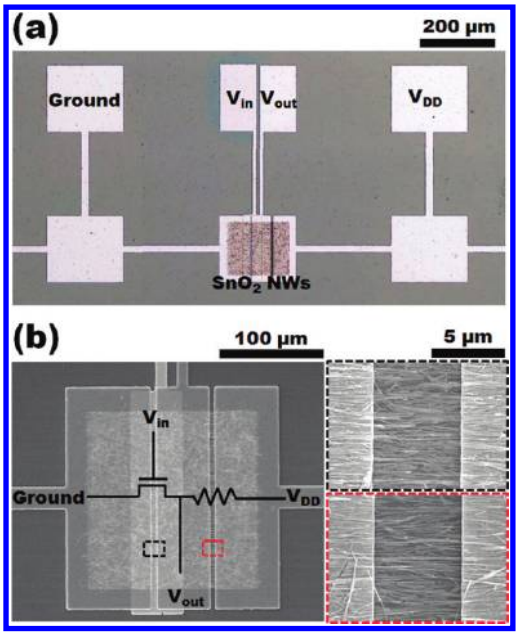

Figure 2. (a) Optical microscope image of an inverter consisting of four electrodes and NW channels. (b) Scanning electron microscope images of the inverter and magnified views of the channels of the FET (dotted black) and resistor (dotted red).

and the FET channels comprised SnO_2 NWs transferred from the as-grown material by a sliding transfer technique.[22] The low adhesion between PI and SiO_2[23] allowed the device arrays to be removed, in their entirety, from the supporting substrates. After the PI

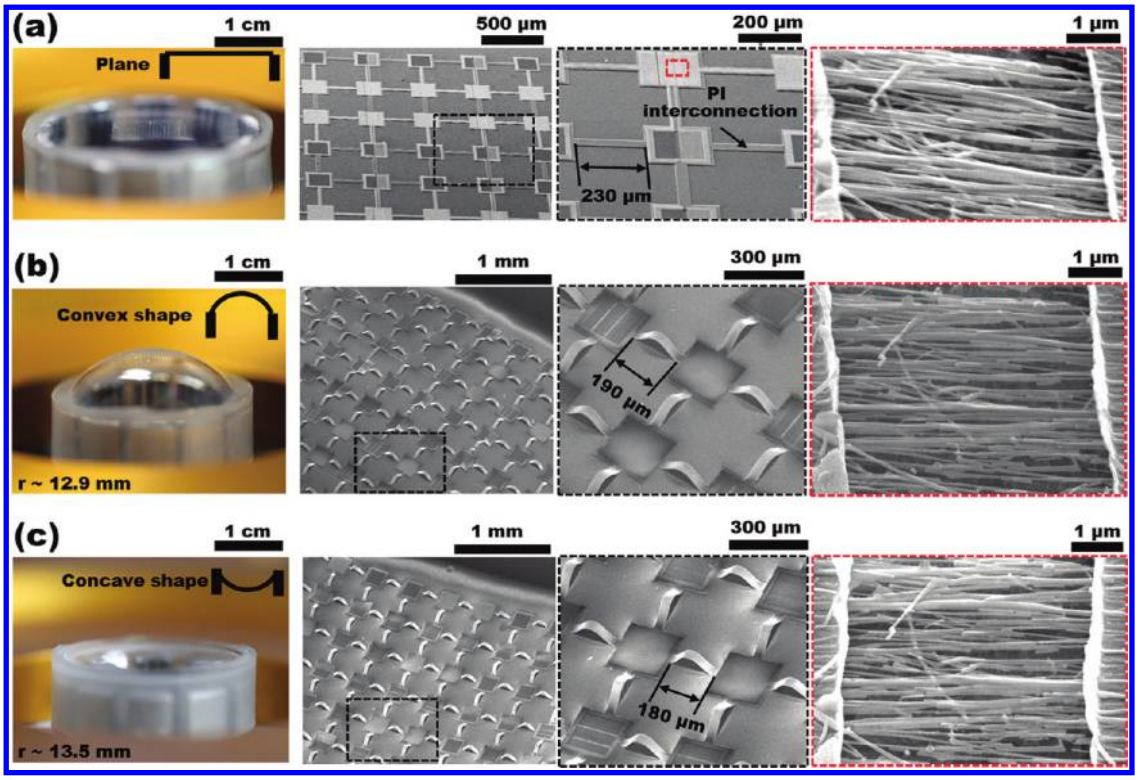

Figure 3. Photographs of the PDMS substrate mounted on a lab-built stretching stage that supports the device arrays in flat and in hemispherical convex/concave shapes (left images). SEM images of the inverter array and suspended SnO_2 nanowires inside the channel on flat (top), hemispherical convex (middle), and concave (bottom) surfaces (right black and white images).

layer was detached from the SiO_2/Si substrate using adhesive tape, it was placed on a polydimethylsiloxane (PDMS) film flattened by a stretching stage. For enhanced deformability, the metal interconnects were formed in narrow geometries; this design allows the integrated mesh to accommodate strains created by relaxing the prestrain, as well as any subsequent deformation, in a way that strain isolates the active devices.[3−7] The narrow interconnects develop into noncoplanar, arc shapes, as they accommodate deformations due to return of the flat, stretched PDMS to its original hemispherical shape. After this transition, it was possible to further deform the system into other different shapes, in a dynamic, reversible fashion. For example, the convex layout could be transformed into an extremely stretched one by externally applied physical force.

An optical microscope image of a representative NW inverter appears in Figure 2a. The inverter consisted of an n-type FET, a resistor with SnO_2 NW channels, and four individual electrodes (V_{DD}, V_{in}, V_{out}, and ground). The electrodes were designed for evaluating the electrical characteristics of the FET, the resistor, and the inverter. After patterning these electrodes by photolithography, SnO_2 NWs were transferred. The presence of aligned NWs was confirmed in the channel and in the device structure by scanning electron microscopy (SEM, Figure 2b). The NWs in the channels of the FET (dotted black) and resistor (dotted red) were aligned along the channel direction perpendicular to the electrodes. The density of NWs directly bridging the electrodes was estimated to be 2−3 NWs/μm in both cases. Some NWs appeared to have been broken during the sliding transfer or lift-off.

An inverter array transferred onto a hemispherical PDMS membrane was stretched with a lab-built stage (Figure 3). The radial tensioning provided by this stage gradually expanded the hemispherical PDMS until flat; its paddle arms mounted into a raised rim formed on the PDMS substrate. The SEM images show that the device morphology changed during transformation into hemispherical convex and concave shapes. Bending radii of hemispherical mold on each shape are indicated in the photographs. When the device array was on a flat film (Figure 3a), that is, no strain on the devices, the devices and their interconnections lie flat on the surface. Releasing the strained PDMS caused the interconnects to adopt arc-shaped geometries, as a consequence of accommodating the strain associated with the shape change (Figure 3b). Because of the relative narrow widths of the interconnections (w = 40 μm) compared to the active device areas (w = 220 μm), the release of surface strain was concentrated at the interconnects. The prestrain was estimated to be *ca.* 21% from the changes (from 230 to 190 μm) of length observed in the SEM images. After converting the convex shape into a concave shape by application of physical force, the average distances between the

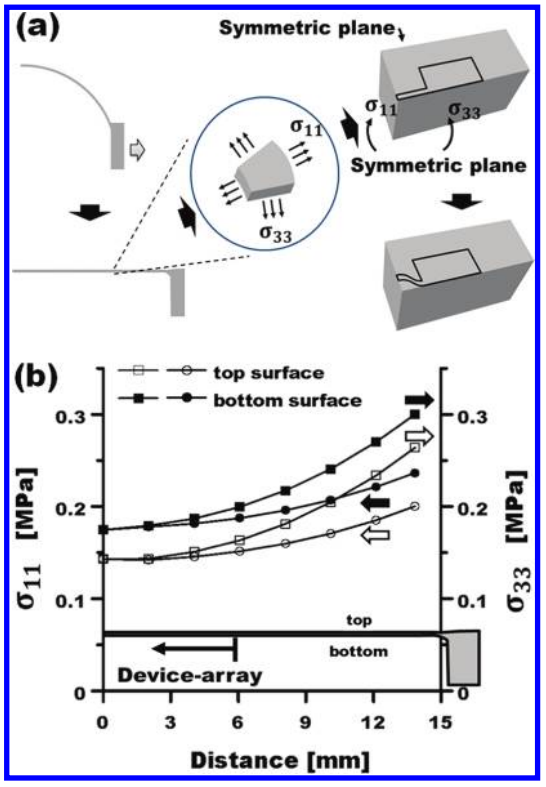

Figure 4. (a) Two-step analysis approach for treating the mechanical deformations; step I analysis of the PDMS substrate and step II analysis of the interaction between the device and the prestressed PDMS substrate; σ_{11} and σ_{33} are the stress in the radial and tangential directions, respectively. (b) Stress development of the PDMS substrate when it was stretched in the radial direction axisymmetrically. Open symbols are for the top surface; σ_{11} (circle) and σ_{33} (square). Closed symbols are for the bottom surface; σ_{11} (circle) and σ_{33} (square).

active devices decreased slightly (from 190 to 180 μm) and the average prestrain increased from 21 to 28%. The top convex surface and the device arrays were compressed on the surface during this transformation. The SEM images of the nanowire region (dotted red) show no noticeable change of nanowire structure across the source/drain electrodes during each transformation.

Understanding the mechanics of such transformations is critically important, particularly for nanowire technologies in suspended geometries such as those used here. The deformations of the device and the interconnects were studied by the finite element method. The mechanical analysis was carried out in two steps: The hemispherical PDMS stretched in the radial direction was analyzed in the first step. The interaction between the device array and the PDMS was analyzed in the second step. The idea of this two-step analysis is shown in Figure 4a. The strain in the PDMS obtained in the first step was transferred to the second step as the prestrain. All components such as the Ti−Au layer, the PI layer, and the PDMS substrate were meshed explicitly. The elastic moduli and the Poisson's ratios of those three materials are 84 000, 2500, and 0.615 MPa and 0.34, 0.33, and 0.5, respectively.[3,24,25] The stress of the PDMS substrate obtained in the step I analysis is shown as Figure 4b, biaxially in the radial (σ_{11}) and the tangential (σ_{33}) directions. The tangential stress was found to be greater than the radial stress at all locations except the center where they were approximately equal. The radial and tangential stresses were in the range of 0.142 to 0.221 MPa and 0.142 to 0.270 MPa, respectively. The difference in the stress between the top and bottom surfaces was due to the bending deformation of the PDMS. The stress at the midsurface of the PDMS was caused by the membrane deformation. As a result, the effect of the bending deformation could be estimated as the ratio of the stress difference between the top and bottom surfaces to the stress at the midsurface. The ratio was about only 10% at the center, while it was even smaller in other places. The magnitude of the prestress is dominated by membrane deformations in the PDMS. Although it might be expected that changing the convex shape to a concave shape would increase the bending contribution up to about 20% if the opposite curvature is assumed, the results show that the membrane deformation still dominates, due partly to the thin geometry of the PDMS membrane. As a result, the effect of the shape change does not need to be included in this mechanical analysis. The strain of the PDMS in the step I analysis was transferred as the prestrain of the PDMS substrate in the step II analysis. Since the whole size of the device array is 8 mm $\times$ 8 mm, the outermost devices reside at positions of less than 6 mm apart from the center of the flattened PDMS.

The deformation of the buckled interconnect during step II analysis is shown in Figure 5a. The distance between the devices was calculated to be between 183 and 185 μm, which agrees with experimentally observed values of 180 to 190 μm. Several positions were chosen to investigate the influence of the prestress of the PDMS substrate in this case, as shown in Figure 5b. The prestress varied from 0.142 to 0.270 MPa. The maximum strain in the interconnect was less than the yield strain of the Ti−Au alloy (~0.18%). The alloy therefore remains in the elastic range after this fabrication process. However, calculations show that, from a distance of 8 mm, the devices can wrinkle due to the high prestress in the tangential direction. The strain of the device in step II analysis is shown in Figure 5c. This strain is compressive if the device is placed within the distance of 6 mm from the center as in this experiment. Figure 5d shows the relative displacement of the device. Because of the compatibility between the PDMS and the device array, the interconnects buckle naturally. Most of the deformations are concentrated at the interconnects, regardless of the position of the device. However, it is found that the device is not entirely free from deformation in the array for certain cases considered in this paper. In particular, the part of

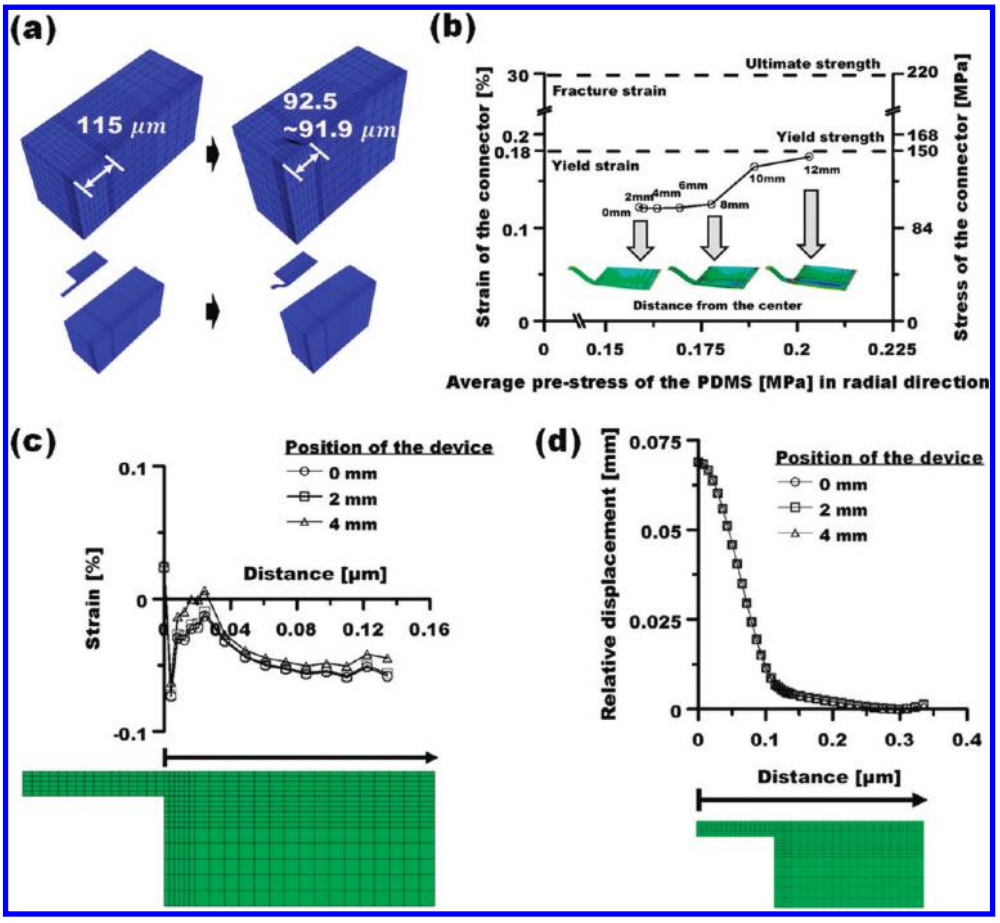

Figure 5. (a) Deformed shape of the system in step II analysis. (b) Stress of the interconnector caused by the release of the PDMS substrate. (c) Strain of the device, evaluated at different positions. (d) Relative displacement of the device, evaluated at different positions. For the magnitude of the prestress at each position, see Figure 4b. The scale of the horizontal axis of (c) and (d) is aligned with a device shown in these figures.

the device near the interconnect deforms as well; see Figure 5d.

In order to confirm the extensive deformability of the device arrays, two different kinds of external force were applied, in ways that are qualitatively different than previous reports which involve much simpler shapes. In Figure 6a, the concave hemisphere of Figure 3c was partially pushed upward with a small PDMS sphere of 8 mm radius. As a result, surfaces with both positive and negative curvatures were created. The SEM images taken over the whole surface show no noticeable difference in the buckling of interconnects between the convex and concave areas, implying an even distribution of strains. On the other hand, the convex hemisphere pushed upward with a small pin of 0.1 mm radius (Figure 6e) yielded SEM images of distinctively different distribution of strains; the fully stretched area around the pushpin exhibit flat interconnects, while the other areas show arc-shaped interconnects as expected. Figure 6h shows the zoomed image of the nanowire region in fully stretched devices. The *I*−*V* curves measured across the fully stretched electrodes (red arrows in Figure 6g) before (distance between electrodes ~190 μm) and after (distance between electrodes ~220 μm) such deformation show no noticeable change of electrical properties, even at such extremes. The stress of the device array when it was pushed upward was calculated by the two-step analysis procedure. The interconnect at the position of the pin exceeded the yield strength because of the highly localized deformation. However, the strain of the device at that position was only 0.10%, which is still elastic. The stress of the device array decreased rapidly by the distance from the pin. In spite of the yielded interconnect, the change of electrical device performance was not noticeable in this case.

Representative electrical properties of the SnO_2 NW FETs are shown in Figure 7a,b. Output characteristics and transfer curves show saturated behavior and strong gate dependence, typical for n-type semiconductor FETs. In this work, the FETs exploited suspended NW channels formed by oxygen plasma etching of underlying PI gate dielectrics. According to our previous report,[23] oxygen plasma can affect both SnO_2 NWs and the underlying PI layer. The depletion region of the SnO_2 NWs can be increased when they are exposed to oxygen plasma due to an increase of

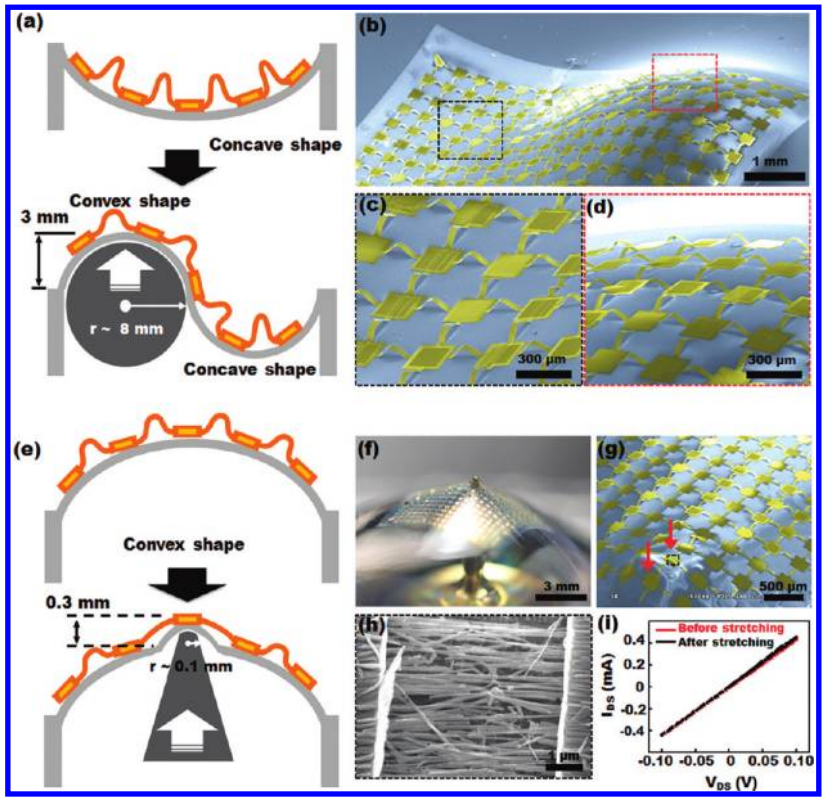

Figure 6. Schematics (a,e) and device images (b−d,f−h) for two different modes of deformation of a hemispherical PDMS substrate. The SEM images were colorized to enhance the contrast between the various regions. Yellow and blue correspond to the device on polyimide and PDMS, respectively. (a) Deformation process from a fully concave shape to a partially concave shape using a spherical implement for applying force. (b−d) SEM images of shapes with both convex and concave areas. (e) Deformation process from fully convex shape to partially stretched convex shape using a pushpin with a small radius of 0.1 mm. (f) Photograph of partially stretched convex PDMS substrate with actual devices. (g,h) SEM images of device and nanowires in extremely stretched region (dotted black). (i) *I*−*V* curve measured across the fully stretched electrodes (red arrows at (h)) before (red) and after (black) deformation.

defects and oxygen vacancies on their surfaces.[26] However, preadsorbed oxygen molecules on the surfaces of NWs are expected to be replaced by water through competitive physisorption of water molecules,[27] under high relative humidity conditions (in our case, RH ~ 50%). Physisorption of water molecules instead of oxygen on the surfaces of NWs with air dielectrics could increase the charge carriers (electrons) to yield stronger gate dependence compared to the FETs with PI dielectrics. The output $I_{DS}-V_{DS}$ curve showed a noticeable variation of current even under a small gate voltage sweep of 0−2 V with 0.2 V step. The current on/off ratio at ±2 V and the on current at +2 V were $>3 \times 10^4$ and *ca.* 3 μA, respectively. Leakage current (I_{GS}) through the gate dielectric was negligible, a few pA. A small threshold voltage (*ca.* 0.7 V) and subthreshold swing (0.2 V/dec) were observed. A near-zero threshold voltage is favorable due to the high gain that are possible at low input voltages (V_{in}). A cylinder on plane model,[28] which considers the summed widths of the total nanowires, allowed the estimation of field effect mobility of the suspended NW FETs to be *ca.* 80 $cm^2/(V \cdot s)$, similar to that in our previous work.[23] As shown in Figure 7b, the electrical performance of the extremely stretched device (red circle) is almost similar to that of the nonstretched device (black triangle). According to the results of Figures 6h and 7b, there seems to be no effective damage in the nanowire devices during extreme stretching transformation. The resistors of the n-FET inverters (n-inverters) consisted of oxygen-plasma-treated SnO_2 NWs. Prior to the oxygen plasma treatment, the SnO_2 NWs had a resistance of *ca.* 300 MΩ, giving an estimated current value at a drain voltage (V_{DD}) of 2 V, similar to or slightly higher than that of the off-state of the FET ($<10^{-10}$ A). Since it is expected that the higher resistance of NW resistor in n-inverters would result in higher gain, we intentionally increased the resistance up to 9 GΩ by plasma treatment (Figure 7c). Figure 7d compares the input−output characteristics of the inverter when the device arrays are on flat and hemispherical convex/concave surfaces. In all cases, the n-inverters exhibited transfer characteristics with a maximum voltage gain of 4.7−4.8 at V_{in} of *ca.* 1.1 V and V_{DD} of 2.0 V. There was no noticeable difference in the inverting properties as the surface changed between flat and hemispherical convex/concave shapes.

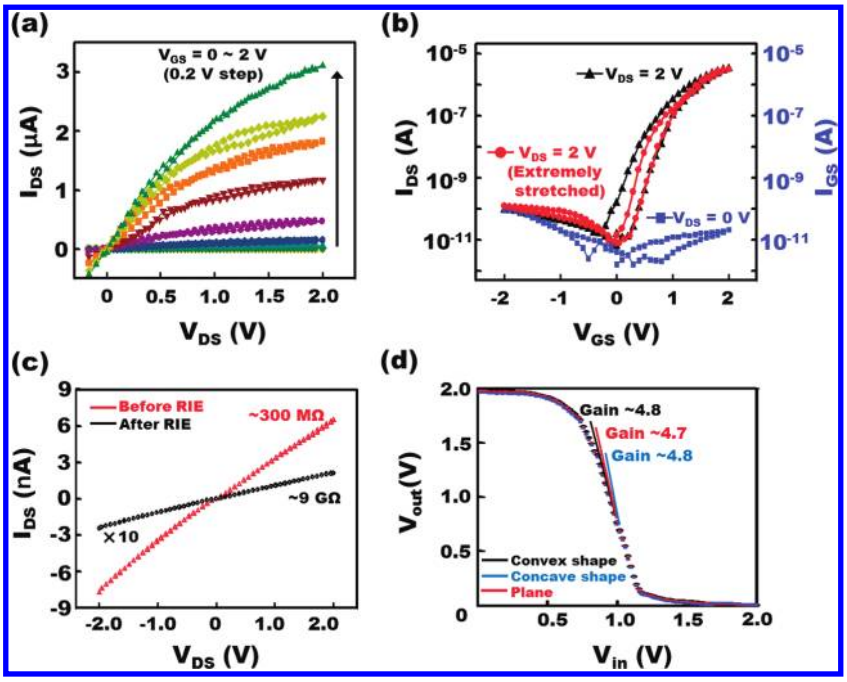

Figure 7. Representative electrical characteristics. (a) Output characteristics and (b) transfer curves of the nonstretched (black triangle) and extremely stretched (red circle) SnO_2 NW FETs (leakage current I_{GS} is shown a blue square). (c) $I-V$ curve of the SnO_2 NW resistor before (red) and after (black) RIE. (d) $V_{out}-V_{in}$ curves of the n-FET inverter on flat (red), hemispherical convex (black), and concave (blue) shape surfaces.

CONCLUSION

In summary, interconnected collections of n-inverters consisting of SnO_2 NW FETs and NW resistors on elastomeric surfaces with a variety of both simple and complex surface shapes, in reversibly deformable configurations, were demonstrated. A two-step analysis scheme revealed the mechanics of deformation during various stages of the fabrication process. It was confirmed from the analysis that the device array remained in an elastic regime of mechanical behavior. The results show that such device arrays, even consisting of fragile, suspended arrays of nanowires, could be reversibly deformed into various shapes without any degradation of electrical performance. This work demonstrates, in a generalized way, that NW technologies can be exploited in mechanically elastic and soft systems, well suited for use in implantable electronics, prosthetics, and other areas such as high-performance sensors where conventional, planar devices cannot meet requirements. The capabilities are expected to complement those reported previously with nanomembrane-based approaches.

METHODS

Growth of SnO_2 Nanowires. SnO_2 nanowires were grown on a SiO_2 substrate using Au catalysts *via* chemical vapor deposition (CVD) method with a vapor−liquid−solid mechanism. Growth conditions were as follows; growth temperature of 750 °C, oxygen flow of 0.5 sccm, processing pressure of ~10^{-2} Torr, and 2 nm thick Au film catalysts.

Device Fabrication. A thin PI layer was coated onto a SiO_2/Si substrate by a previously reported procedure.[23] After depositing the V_{in} electrode, a second PI layer, used as a temporary gate insulator, was coated onto the substrate. SnO_2 NWs, synthesized by chemical vapor deposition, were contact-transferred from a donor substrate to an acceptor substrate using a lab-built sliding transfer machine.[22] Both the donor and acceptor substrates were slid in opposite directions at a speed of 20 mm/min under an applied pressure of 0.5 kg/cm^2. Ti and Au were evaporated to fabricate the V_{DD}, V_{out}, and source (ground) electrodes, which defined the nanowire channel length and width as 5 and 160 μm, respectively. When the PI layer was exposed to O_2 plasma, NWs were suspended as the underlying PI layer was etched. The PI layers directly beneath the NWs were completely removed within 7 min of etching with an O_2 gas flow rate of 20 sccm, at a pressure of 50 mTorr, and RF power of 150 W.

Hemispherical PDMS Molding. An aluminum jig and hemispherical convex and concave PDMS were used for molding the hemispherical thin film.[3−7] The hemispherical thin film was molded in the small gap between the concave and convex PDMS. The PDMS mold was prepared with a raised rim around its perimeter. Vertically fitted paddle arms of the lab-built stretchable stage stretched the raised rim of the hemispherical PDMS to flatten it.

Mechanical Analysis. Commercial finite element code ABAQUS was used for the analysis. Step I analysis was an axisymmetric analysis with quadratic elements. Step II analysis was a three-dimensional analysis. The result of the step I analysis was used for the initial condition of the step II analysis. The PDMS and the device array were meshed by using a linear brick element and a quadratic brick element, respectively. The PDMS and the device except the interconnector were tied together. A prestress for the step II analysis was implemented by using a user-supplied subroutine.

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